NISTTech

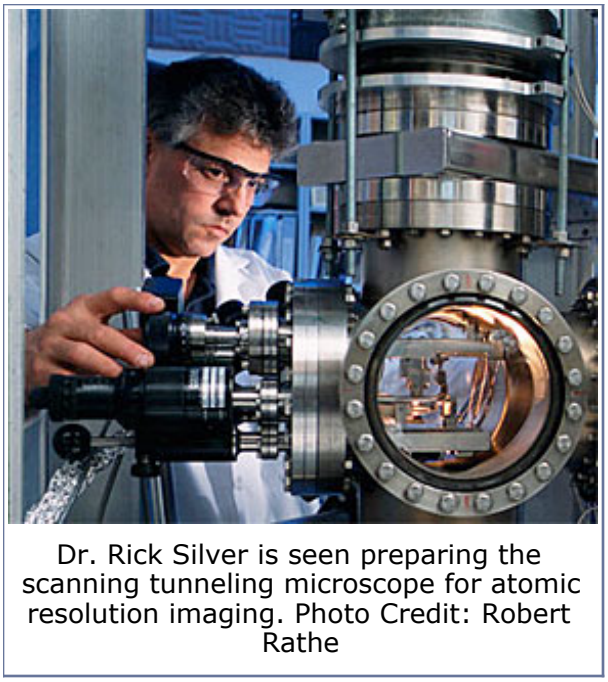
Zero Order Overlay Targets for Semiconductors

Overlay targets that reduce defects in semiconductor manufacturing

Description

Reduce defects in semiconductor fabrication by using overlay measurements and targets to tightly control layer-to-layer alignment. The new method uses slightly different overlay targets on each layer of a semiconductor structure. The targets consist of finely-spaced parallel lines, each having a slightly different spacing or pitch, thus enabling optical scans to determine overlay error.

Images



Dr. Rick Silver is seen preparing the scanning tunneling microscope for atomic resolution imaging. Photo Credit: Robert Rathe

Applications

- **Semiconductor manufacturing**
  Used in semiconducting manufacturing to determine and correct overlay errors, resulting in structures that have approximately perfect overlay or alignment, thereby reducing the potential for defects that can cause short circuits and connection failures.

Advantages

- **Flexible**
  Not limited to particular manufacturing processes or machines, means, methods or steps that perform essentially the same function or achieve the same results. No limitations on feature size and density.
- **Diverse applications**
  Allows optical overlay measurements to be performed using device-sized dimensions and very dense targets.
- **Easy to implement**
  Uses conventional imaging techniques.

Abstract

A zero-order overlay target comprises a first zero-order line array fabricated on a first layer of a semiconductor structure, the first zero-order line array having a first pitch, and a second zero-order line array fabricated on a second layer of the semiconductor structure, the second zero-order line array having a second pitch. The second pitch may be different from the first pitch, and a portion of the second zero-order line array may be positioned to become optically coupled to a portion of the first zero-order line array when subject to an overlay measurement. Further, the second pitch may be variable. For example, the variable pitch may comprise a first set of features having a pitch approximately equal to the first pitch, a second set of features having a pitch different from the first pitch, and a third set of features having a pitch approximately equal to the first pitch.

Inventors

- Attota, Ravikiran
- Barnes, Brian
- Silver, Richard M.
- Lipscomb, Pete

Citations

1. R.M. Silver, R. Attota, and E. Marx. Model-based analysis of the limits of optical metrology with experimental comparisons. Proceedings of SPIE, Vol 6617, pp. 13, January 2007.
2. Y.J. Sohn, B.M. Barnes, L. Howard, R.M. Silver, R. Attota, and M.T. Stocker. Köhler Illumination for High-resolution Optical Metrology Proc. SPIE 6518, 65184V (2007); doi:10.1117/12.714890.

References

- U.S. Patent Application # 20080142998

- Docket: 07-002

Status of Availability

This invention is available for licensing.

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